IN THE CLAIMS

Please amend the claims as follows:

1 – 13. (Cancelled)

14. (New) A semiconductor device, comprising on a same semiconductor substrate, a first MIS type transistor and a second MIS type transistor having a same conductivity type as the first MIS type transistor, wherein:

the first MIS type transistor comprises:

a first gate insulating film formed on a first transistor-forming region in the semiconductor substrate;

a first gate electrode formed on the first gate insulating film;

first sidewall insulating films formed on side surfaces of the first gate electrode;

first low concentration impurity regions formed underneath the first sidewall insulating films in the first transistor-forming region;

first high concentration impurity regions formed outside the first gate electrode in the first transistor-forming region so as to adjoin to the first low concentration impurity regions; and

first metal silicide layers formed on each surface of the first high concentration impurity regions using the first sidewall insulating films as a mask, and

the second MIS type transistor comprises:

a second gate insulating film formed on a second transistor-forming region in the semiconductor substrate and having a thickness thinner than the first gate insulating film;

a second gate electrode formed on the second gate insulating film;

second sidewall insulating films formed on side surfaces of the second gate electrode;

second low concentration impurity regions formed underneath the second sidewall insulating films in the second transistor-forming region;

second high concentration impurity regions formed outside the second gate electrode in the second transistor-forming region so as to adjoin to the second low concentration impurity regions;

third sidewall insulating films formed on the portions of the second high concentration impurity regions located in proximity of the second low concentration impurity regions and on the side surfaces of the second sidewall insulating films; and

second metal silicide layers formed on each surface of the second high concentration impurity regions using the second sidewall insulating films and the third sidewall insulating films as a mask

15. (New) The semiconductor device according to claim 14, wherein:

the second metal silicide layer is provided on the surface of the second high concentration impurity region except for its portion located underneath the third sidewall insulating film.

16. (New) The semiconductor device according to claim 14, wherein:

the depth of the second high concentration impurity regions except for their portions located underneath the third sidewall insulating films are deeper than the depth of the portions of the second high concentration impurity regions located underneath the third sidewall insulating films.

17. (New) The semiconductor device according to claim 14, wherein:

the first and second sidewall insulating films are made of first insulating film; and

the third sidewall insulating films are made of second insulating film.

18. (New) The semiconductor device according to claim 14, wherein:

the device further comprises a silicidization-preventing pattern formed on the top side of a resistance element-forming region in the second high concentration impurity region; and

the second metal silicide layer is provided on the surface of the second high concentration impurity region except for its portion located underneath the third sidewall insulating film and the silicidization-prevention pattern.

19. (New) The semiconductor device according to claim 18, wherein:

the depth of the second high concentration impurity regions except for their portions located underneath the third sidewall insulating films and the silicidization-preventing pattern are deeper than the depth of the portions of the second high concentration impurity regions located underneath the third sidewall insulating films and the silicidization-preventing pattern.

20. (New) The semiconductor device according to claim 18, wherein:

the first and second sidewall insulating films are made of first insulating film; and

the third sidewall insulating films and the silicidization-preventing pattern are made of second insulating film.

21. (New) The semiconductor device according to claim 14, wherein:

the first sidewall insulating films are formed on first offset spacers formed on the side surfaces of the first gate electrode.

22. (New) The semiconductor device according to claim 14, wherein:

the second sidewall insulating films are formed on second offset spacers formed on the side surfaces of the second gate electrode.

23. (New) The semiconductor device according to claim 14, wherein:

the first metal silicide layer is formed on the top surface of the first gate electrode; and

the second metal silicide layer is formed on the top surface of the second gate electrode.

24. (New) The semiconductor device according to claim 14, wherein:

the first MIS type transistor is an internal transistor; and

the second MIS type transistor is an input/output transistor.